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10/588,636	08/04/2006	Kazuyoshi Okawa	NAA243	9797

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EXAMINER	
MCMAHON, DANIEL F	

ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/588,636	OKAWA ET AL.	
	Examiner	Art Unit	
	DANIEL F. MCMAHON	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to amendments filed January 6, 2009.

Claims 1—7 and 9 – 10 have been amended.

Claims 1 – 10 are pending.

Response to Amendment

1. The objection to the specification is withdrawn in light of the amendments to the claims.

Response to Arguments

2. Applicant's arguments, filed January 06, 2009 regarding claims 1 – 10, have been fully considered but they are not persuasive.

Regarding Stallman, Applicant argues 'hooks' as disclosed in Stallman are not capable of transforming Emacs into a program with new capabilities. Stallman discloses 'hooks' as a method to transform Emacs in anyway the programming language Lisp will allow, "You can use any valid Lisp function as the hook function" (section 30.2.3 Hooks page 1, line 14).

Applicant argues "Stallman has nothing to do with memory analysis and repair". 'hooks' as disclosed by Stallman are a very well known technique in the art of programming. The ability to customize behavior of a program based on user input is applicable to the creation and execution of computer programs in general. 'hooks' may

be used to customize the behavior of a computer program based on user input (section 30.2.3 Hooks, paragraph 3).

3. Regarding claim 4, applicant argues: figure 1, element 20 of Oikawa does not teach the repair analysis computing unit. As claimed, the repair analysis computing unit (figure 1, element 20) as taught by Oikawa is capable of performing repair analysis (column 8, lines 28 - 36).

4. Regarding claim 5, applicant argues: figure 1, element 10 of Oikawa does not teach the analysis program storage section. Oikawa teaches the analysis program storage section as part of work station 10 (column 5, lines 36 – 55, lines 57 - 59).

5. Regarding claim 10, applicant argues Oikawa does not teach the limitation of "selecting a set of user functions that correspond to the type of the semiconductor device under test from among a plurality of sets of user functions". Oikawa explicitly teaches the "selecting of a set of user functions that correspond to the type of the semiconductor device under test from among a plurality of sets of user functions" (column 8, lines 28 – 30).

Prior Art Rejections

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 2, 4 – 7, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oikawa et al. U.S. Patent 6,459,292 (herein Oikawa), in view of "GNU Emacs 19 Manual" by Richard M. Stallman (herein Stallman).

9. Regarding claim 1, Oikawa teaches: a semiconductor device test apparatus (abstract): a test processor which applies a test signal to a semiconductor device under test and obtains information about a defective memory cell from a response signal (figure 1, element 20); and a repair analysis computing unit which performs repair analysis of the defective memory cell information to determine a way to repair the defective memory cell (figure 1, element 50 – 5F); wherein the repair analysis

computing unit comprises: memory repair analysis means for performing repair analysis of the defective memory cell information in accordance with a memory repair analysis program based on regular defective memory cell repair conditions that are applicable to a regular type semiconductor device having a regular type memory structure and determining assignment of a spare line to the defective memory cell (column 6, lines 32 – 43), said memory repair analysis program comprising operations constituting a process of repair analysis of the defective memory cell information (column 8, lines 28 – 36) said memory repair analysis means performs repair analysis of the defective memory cell information based on specific defective memory cell repair conditions that are applicable to a specific type of semiconductor device having a specific type memory structure other than the regular type memory structure (column 8, lines 28 – 36).

Oikawa does not teach: a user function means for inserting user functions of a user-specified user analysis program to user function insertion points between operations of the memory repair analysis program to make a change to data processed by the memory repair analysis program.

Stallman teaches: a user function means for inserting user functions of a user-specified user analysis program to user function insertion points between operations of the memory repair analysis program to make a change to data processed by the memory repair analysis program (section 30.2.3 Hooks, paragraph 1 – 3).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Oikawa: a test processor and repair analysis computing unit with memory repair analysis means, with the teaching of Stallman: a

user function means, for the purpose of allowing the user to customize behavior of the mode of the memory repair analysis program (section 30.2.3 Hooks, paragraph 3, lines 1 - 2).

10. Regarding claim 2, Oikawa and Stallman teach the limitations of the parent claim, claim 1. Oikawa does not teach: memory repair analysis public function means for inserting the user functions to the user function insertion points through the intervention of a memory repair analysis public function.

Stallman teaches: memory repair analysis public function means which inserts the user function between desired units of processing of the memory repair analysis program through the intervention of a memory repair analysis public function (section 30.2.3 Hooks, paragraph 1 – 3).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Oikawa: as cited above, with the teaching of Stallman: a memory repair analysis public function means, for the purpose of allowing the user to customize behavior of the mode of the memory repair analysis program (section 30.2.3 Hooks, paragraph 3, lines 1 - 2).

11. Regarding claim 4, Oikawa and Stallman teach the limitations of the parent claim, claim 1. Oikawa additionally teaches: a fail memory which stores the defective memory cell information from the test processor (figure 1, element 60 – 6F; column 6, lines 12 – 14); a memory repair analysis program storage section which stores the memory repair

analysis program (figure 1, element 41 – 44); a user analysis program storage section which stores the user analysis program; and an analysis control part which controls execution of the memory repair analysis program and execution of the user analysis program (figure 1, element 20); and the analysis control part and the memory repair analysis program storage section constitute the memory repair analysis means and the analysis control part and the user analysis program storage section constitute the user function means (figure 1).

12. Regarding claim 5, Oikawa and Stallman teach the limitations of the parent claim, claim 5. Oikawa additionally teaches: a repair condition file storage section which stores a plurality of repair condition files, each defining a repair condition for each type of semiconductor device (column 8, lines 28 – 36, 52 – 56); the user analysis program storage section stores as the user analysis program a plurality of sets of user functions defined correspondingly to the plurality of repair condition files (figure 1, element 10); and the analysis control part selects a set of user functions on the basis of a repair condition file that matches the type of the semiconductor device under test and (column 8, lines 52 – 56). Oikawa does not teach: inserting the set of user functions to the user function insertion points.

Stallman teaches: inserting the set of user functions to the user function insertion points (section 30.2.3 Hooks, paragraph 1 – 3).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Oikawa: as cited above, with the teaching of

Stallman: inserting the set of user functions, for the purpose of allowing the user to customize behavior of the mode of the memory repair analysis program (section 30.2.3 Hooks, paragraph 3, lines 1 - 2).

13. Regarding claim 6, Oikawa teaches: a semiconductor device test method (abstract) (a) performing a function test on a memory of a semiconductor device under test to obtain information about a defective memory cell (abstract); (b) performing repair analysis of the defective memory cell information in accordance with a memory repair analysis program which comprises operations constituting a process of repair analysis of the defective memory cell information based on regular defective memory cell repair conditions that are applicable to a regular type semiconductor device having a regular type memory structure to determine assignment of a spare line to the defective memory cell (column 6, lines 32 – 43; column 8, lines 28 – 36); and (c) using functions based on a user-defined defective memory cell repair condition to make a change to data processed by the memory repair analysis program so that repair analysis of the defective memory cell information is performed based on specific defective memory cell repair condictions that are applicable to a specific type semiconductor device having a specific type memory structure other than the regular type memory structure (column 8, lines 28 – 36, 52 – 56). Oikawa does not teach: inserting a user function between desired processing units.

Stallman teaches: inserting a user function between desired processing units (section 30.2.3 Hooks, paragraph 1 – 3).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Oikawa: performing a function test on a memory and performing memory repair analysis, as cited above, with the teaching of Stallman: inserting a user function, for the purpose of allowing the user to customize behavior of the mode of the memory repair analysis (section 30.2.3 Hooks, paragraph 3, lines 1 - 2).

14. Regarding claim 7, Oikawa and Stallman teach the limitations of the parent claim, claim 6. Oikawa does not teach: inserting the user function to the4 user function insertion points through intervention of a memory repair analysis public function.

Stallman teaches: inserting the user function between units of processing of the memory repair analysis program through the intervention of a memory repair analysis public function (section 30.2.3 Hooks, paragraph 1 – 3).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Oikawa: as cited above, with the teaching of Stallman: a public function, for the purpose of allowing the user to customize behavior of the mode of the memory repair analysis (section 30.2.3 Hooks, paragraph 3, lines 1 - 2).

15. Regarding claim 9, Oikawa and Stallman teach the limitations of the parent claim, claim 6. Oikawa additionally teaches: performing line fail repair processing and performing bit repair processing (column 6, lines 32 – 43). Oikawa does not teach: making a change to the result of the line fail repair processing through the user function after the step of performing the line fail repair processing and the step of making a

change to the result of the bit repair processing through the user function after the step of performing the bit repair processing.

Stallman teaches: making a change to the result of the line fail repair processing through the user function after the step of performing the line fail repair processing and the step of making a change to the result of the bit repair processing through the user function after the step of performing the bit repair processing (section 30.2.3 Hooks, paragraph 1 – 3).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Oikawa: performing line fail repair processing and performing bit repair processing, as cited above, with the teaching of Stallman: the user function inserted between program steps, for the purpose of allowing the user to customize behavior of the mode of the memory repair analysis (section 30.2.3 Hooks, paragraph 3, lines 1 - 2).

16. Regarding claim 10, Oikawa and Stallman teach the limitations of the parent claim, claim 6. Oikawa additionally teaches: selecting a set of functions that corresponds to the type of the semiconductor device under test from among a plurality of sets of user functions provided correspondingly to a plurality of repair conditions predetermined for the types of semiconductor devices and inserting the set of user functions to the user function insertion points (column 8, lines 28 – 36, 52 – 56).

17. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oikawa and Stallman, in view of Reese, U.S. Patent 6,370,516 (herein Reese).

18. Regarding claim 3, Oikawa and Stallman teach the limitations of the parent claim, claim 2. Oikawa does not teach: memory repair analysis public function having a data check function portion which checks data set by the user function to determine whether the data is proper.

Reese teaches: having a data check function portion which checks whether data set by the user is proper (claim 18).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Oikawa: as cited above, and the teaching of Reese: a data check function, for the purpose of maintaining proper operation of software. A data check function is a well known technique and the combination would yield predictable results.

19. Regarding claim 8, Oikawa and Stallman teach the limitations of the parent claim, claim 7. Oikawa does not teach: executing a data check function which checks data set by the user function to determine whether the data is proper.

Reese teaches: executing a data check function which checks data set by the user function to determine whether the data is proper (claim 18).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Oikawa: as cited above, and the teaching of

Reese: a data check function, for the purpose of maintaining proper operation of software. A data check function is a well known technique and the combination would yield predictable results.

Conclusion

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL F. MCMAHON whose telephone number is (571)270-3232. The examiner can normally be reached on M-Th 8am-5pm(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571)272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cynthia Britt/
Primary Examiner, Art Unit 2117

Dfm
03/25/2009